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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,766	10/23/2001	Ralph C. Tuttle	5000.142	3061

21176 7590 12/29/2003

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EXAMINER	
STEVENSON, ANDRE C	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 12/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,766	TUTTLE ET AL.	
	Examiner	Art Unit	
	Andre' C. Stevenson	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) *28-43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8,11,12,18,21-23,25 and 26* is/are rejected.

7)☒ Claim(s) *4,5,9,10,13-17,19,24 and 27* is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim #1 through 3, 6 through 8, 11, 12, 18, 21 through 23, 25 and 26 are rejected under 35 U.S.C. 102(a) as being unpatentable over Rostoker et al (U.S. Pat. No.5811863).

Rostoker et al (U.S. Pat. No.5811863), **Claim #1**, a labeled semiconductor material comprising: a surface of a semiconductor material; and a first metal layer on portions but not all of said surface; said metal layer forming a pattern with rotational symmetry of C_n, where n is at least 2, (Fig. 20, Column 92, lines 27 through 29, Column 93, lines 12 through 15, Column 94, lines 22 through 24, Column 15, lines 1 through 16, Column 16, lines 4 through 22)

Furthermore, **Claim #2**, a labeled semiconductor according to Claim 1 and further comprising: a second metal layer on portions but not all of said surface of said

semiconductor material; said second metal layer forming a pattern different from said first metal layer pattern; and said second pattern having rotational symmetry of C_n where n is at least 2, is taught by Rostoker et al (U.S. Pat. No.5811863) (column 16, line 4 through 22).

With respect to **Claim #3,** a method of claim 1 further comprising removing less than about 200 Angstroms per minute from the semiconductor test wafer, is taught by Rostoker et al (U.S. Pat. No.5811863) (Column 9, lines 24 through 39).

Considering now **Claim #4,** a method of claim 1 further comprising removing less than about 200 Angstroms per minute from the semiconductor test wafer, is taught by Rostoker et al (U.S. Pat. No.5811863) (Column 9, lines 24 through 39).

Furthermore, **Claim #2**, a labeled semiconductor according to Claim 1 and further comprising: a second metal layer on portions but not all of said surface of said semiconductor material; said second metal layer forming a pattern different from said first metal layer pattern; and said second pattern having rotational symmetry of C_n where n is at least 2, is taught by Rostoker et al (U.S. Pat. No.5811863) (column 8, line 28 through 49).

With respect to **Claim #3,** a labeled semiconductor according to Claim 2 wherein portions of said second metal layer overlie portions of said first metal layer, is taught by Rostoker et al (U.S. Pat. No.5811863) (Column 9, lines 24 through 39).

Considering now **Claim #6,** a labeled semiconductor according to Claim 1 wherein said C,, pattern includes linearly sequential metallized and non-metallizcd portions, is taught by Rostoker et al (U.S. Pat. No.5811863) (Fig. 2, Column 13, lines 58 through 67, Column 14, lines 1 through 15).

Furthermore, **Claim #7**, a labeled semiconductor according to Claim 2 wherein said first and second metal layers comprise concentric circles, is taught by Rostoker et al (U.S. Pat. No.5811863) (column 15, line 17 through 29, Column 17, lines 1 through 11, Column 82, lines 40 through 44, lines 52 through 65).

With respect to **Claim #8, a** labeled semiconductor according to Claim 1 wherein said metal layers form an ohmic contact to said semiconductor material, is taught by Rostoker et al (U.S. Pat. No.5811863) (Column 2, lines 29 through 40).

Considering now **Claim #11,** a semiconductor structure comprising: a substrate having at least one planar face; a first metal layer on said planar face, and covering some, but not all of said planar face in a first predetermined geometric pattern; and a second metal layer on said planar face, and covering some, bat not all of said planar

face in a second geometric pattern that is different from said first geometric pattern, is taught by Rostoker et al (U.S. Pat. No.5811863) (Column 9, lines 24 through 39).

Furthermore, **Claim #12**, a semiconductor structure according to Claim 11 wherein portions of said second metal layer overlie portions of said first metal layer, is taught by Rostoker et al (U.S. Pat. No.5811863) (column 8, line 28 through 49).

With respect to **Claim #18,** a semiconductor structure according to Claim 11 wherein said first and second geometric patterns have C_n rotational symmetry where n is at least 2, is taught by Rostoker et al (U.S. Pat. No.5811863) (Column 9, lines 24 through 39).

Considering now **Claim #20,** a semiconductor wafer comprising: respective primary and secondary orthogonal flats; respective front and back planar faces; a plurality of devices on said wafer; each said device having a first metal layer on said planar face, and covering some, but not all of said planar face in a first predetermined geometric pattern; and each said device having a second metal layer on said planar face, and covering some, but not all of said planar face in a second geometric pattern that is different from said first geometric pattern, is taught by Rostoker et al (U.S. Pat. No.5811863) (Column 9, lines 24 through 39).

Furthermore, **Claim #21**, a semiconductor wafer according to Claim 20 wherein the devices on said wafer are identical to one another, is taught by Rostoker et al (U.S. Pat. No.5811863) (column 8, line 28 through 49).

With respect to **Claim #22,** a semiconductor wafer according to Claim 20 wherein said devices are aligned in a predetermined relationship with said flats, is taught by Rostoker et al (U.S. Pat. No.5811863) (Column 9, lines 24 through 39).

Considering now **Claim #23,** a semiconductor wafer according to Claim 20 wherein said first and second patterns have Cn rotational symmetry where n is at least 2., is taught by Rostoker et al (U.S. Pat. No.5811863) (Column 9, lines 24 through 39).

Furthermore, **Claim #25**, a semiconductor wafer according to Claim 20 wherein said metal layers form respective ohmic contacts to said devices, is taught by Rostoker et al (U.S. Pat. No.5811863) (column 8, line 28 through 49).

With respect to **Claim #26,** a semiconductor wafer according to Claim 20 wherein said devices are selected from the group consisting of: junction diodes, bipolar transistors, thyristors, MESFETS, NETS, MOSFETs and photodetectors, is taught by Rostoker et al (U.S. Pat. No.5811863) (Column 9, lines 24 through 39).

Objected Claims

Claims 4, 5, 9, 10, 13 through 17, 19, 24 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 4 and 5

- Second patterns forms an X pattern.

Claims 9 and 10

- Comprising silicon carbide.

Claims 13 through 17 and 19

- Epitaxial layer on the oppsite side of said substrate from said planar face and said metal layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre' Stevenson whose telephone number is (703) 308 6227. The examiner can normally be reached on Monday through Friday from 7:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached on (703) 308 3325. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308

0956. Also, the proceeding numbers can be used to fax information through the Right Fax system;

- **(703) 872 - 9306**

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800

Andre' Stevenson

Art Unit 2812

12/18/03